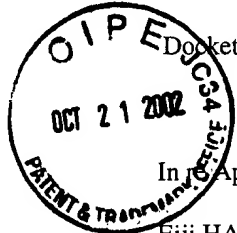


AF 11725



Docket No.: 50088-056

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Application of

: Response Under 37 CFR 1.116 - Expedited Procedure

Eiji HAYASHI

Serial No.: 09/810,454

: Group Art Unit: 1725

Filed: March 19, 2001

: Examiner: Jonathan J. Johnson

For: FLIP CHIP BONDING METHOD

Box AF
THE COMMISSIONER FOR PATENTS AND TRADEMARKS
Washington, DC 20231

Dear Sir:

Transmitted herewith is an Amendment in the above identified application.

- ☒ No additional fee is required.
☐ Applicant is entitled to small entity status under 37 CFR 1.27
☐ Also attached:

The fee has been calculated as shown below:

	NO. OF CLAIMS	HIGHEST PREVIOUSLY PAID FOR	EXTRA CLAIMS	RATE	FEE
Total Claims	4	20	0	\$18.00 =	\$0.00
Independent Claims	3	3	0	\$84.00 =	\$0.00
Multiple claims newly presented					\$0.00
Fee for extension of time					\$0.00
Total of Above Calculations					\$0.00

- ☐ Please charge my Deposit Account No. 500417 in the amount of \$0.00. An additional copy of this transmittal sheet is submitted herewith.
- ☒ The Commissioner is hereby authorized to charge payment of any fees associated with this communication or credit any overpayment, to Deposit Account No. 500417, including any filing fees under 37 CFR 1.16 for presentation of extra claims and any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

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Docket No.: 50088-056



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TC 1700

#6/B 10/25/02
DEF 9)
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Eiji HAYASHI

Serial No.: 09/810,454

Filed: March 19, 2001

For: FLIP CHIP BONDING METHOD

: RESPONSE UNDER 37 CFR § 1.116

: EXPEDITED PROCEDURE

: Group Art Unit: 1725

: Examiner: Jonathan J. Johnson

AMENDMENT UNDER 37 CFR § 1.116

Box AF
Commissioner for Patents
Washington, DC 20231

Sir:

The following Amendments and Remarks are filed in response to the Office Action dated August 12, 2002, pursuant to 37 C.F.R. § 1.116.

IN THE CLAIMS:

Please add new claims 3 and 4 as follows:

3. A flip chip bonding method for mounting a semiconductor element on a wiring board comprising steps of:

applying a vacuum to the semiconductor element through an ultrasonic bonding head to fixedly attach the semiconductor element to the ultrasonic bonding head; and

applying a pressure and heat to solder bumps, formed on both or one of a connecting pad of the semiconductor element or a connecting pad of the wiring board for connecting the solder bumps